Ultralow Distortion Differential ADC Driver

ADA4938-1/ADA4938-2

FEATURES

- Extremely low harmonic distortion
  - −106 dBc HD2 @ 10 MHz
  - −82 dBc HD2 @ 50 MHz
  - −109 dBc HD3 @ 10 MHz
  - −82 dBc HD3 @ 50 MHz
- Low input voltage noise: 2.6 nV/√Hz
- High speed
  - −3 dB bandwidth of 1000 MHz, G = +1
  - Slew rate: 4700 V/µs
  - 0.1 dB gain flatness to 150 MHz
  - Fast overdrive recovery of 4 ns
- 1 mV typical offset voltage
- Externally adjustable gain
- Differential-to-differential or single-ended-to-differential operation
- Adjustable output common-mode voltage
- Wide supply voltage range: +5 V to ±5 V
- Single or dual amplifier configuration available

APPLICATIONS

- ADC drivers
- Single-ended-to-differential converters
- IF and baseband gain blocks
- Differential buffers
- Line drivers

GENERAL DESCRIPTION

The ADA4938 is a low noise, ultralow distortion, high speed differential amplifier. It is an ideal choice for driving high performance ADCs with resolutions up to 16 bits from dc to 27 MHz, or up to 12 bits from dc to 74 MHz. The output common-mode voltage is adjustable over a wide range, allowing the ADA4938 to match the input of the ADC. The internal common-mode feedback loop also provides exceptional output balance as well as suppression of even-order harmonic distortion products.

Full differential and single-ended-to-differential gain configurations are easily realized with the ADA4938. A simple external feedback network of four resistors determines the closed-loop gain of the amplifier.

The ADA4938 is fabricated using the Analog Devices, Inc. proprietary third-generation, high voltage XFCB process, enabling it to achieve very low levels of distortion with an input voltage noise of only 2.6 nV/√Hz. The low dc offset and excellent dynamic performance of the ADA4938 make it well suited for a wide variety of data acquisition and signal processing applications.

FUNCTIONAL BLOCK DIAGRAMS

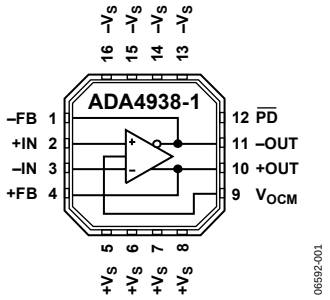

Figure 1. ADA4938-1 Functional Block Diagram

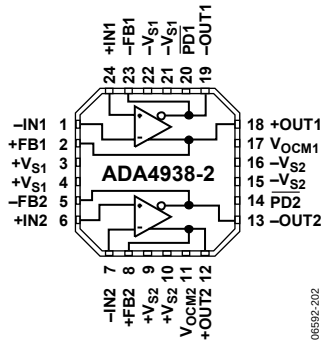

Figure 2. ADA4938-2 Functional Block Diagram

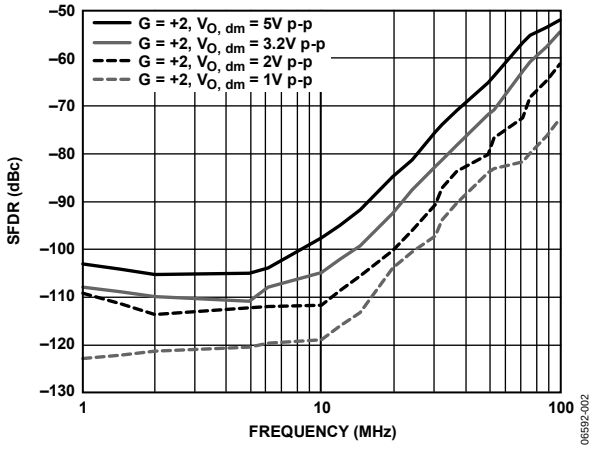

Figure 3. SFDR vs. Frequency and Output Voltage

The ADA4938-1 (single amplifier) is available in a Pb-free, 3 mm × 3 mm, 16-lead LFCSP. The ADA4938-2 (dual amplifier) is available in a Pb-free, 4 mm × 4 mm, 24-lead LFCSP. The pinouts have been optimized to facilitate layout and minimize distortion. The parts are specified to operate over the extended industrial temperature range of −40°C to +85°C.

Rev. 0

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REVISION HISTORY

11/07—Revision 0: Initial Version

SPECIFICATIONS

DUAL-SUPPLY OPERATION

T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = −5 V, V_{OCM} = 0 V, R_T = 61.9 Ω, R_G = R_F = 200 Ω, G = +1, $R_{L, dm}$ = 1 kΩ, unless otherwise noted.
All specifications refer to single-ended input and differential output, unless otherwise noted. For gains other than G = 1, values for R_F and R_G are shown in Table 11.

Table 1. ±D_{IN} to ±OUT Performance

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	V_{OUT} = 0.1 V p-p		1000		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 2 V p-p		150		MHz
Large Signal Bandwidth	V_{OUT} = 2 V p-p		800		MHz
Slew Rate	V_{OUT} = 2 V p-p		4700		V/µs
Overdrive Recovery Time	V_{IN} = 5 V to 0 V step, G = +2		4		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	V_{OUT} = 2 V p-p, 10 MHz		−106		dBc
	V_{OUT} = 2 V p-p, 50 MHz		−82		dBc
Third Harmonic	V_{OUT} = 2 V p-p, 10 MHz		−109		dBc
	V_{OUT} = 2 V p-p, 50 MHz		−82		dBc
IMD	f_1 = 30.0 MHz, f_2 = 30.1 MHz		89		dBc
IP3	f = 30 MHz, $R_{L, dm}$ = 100 Ω		45		dBm
Input Voltage Noise	f = 10 MHz		2.6		nV/√Hz
Noise Figure	G = +4, f = 10 MHz		15.8		dB
Input Current Noise	f = 10 MHz		4.8		pA/√Hz
Crosstalk (ADA4938-2)	f = 100 MHz		−85		dB
INPUT CHARACTERISTICS					
Offset Voltage	$V_{OS, dm} = V_{OUT, dm}/2$; $V_{DIN+} = V_{DIN-}$ = 0 V		1	4	mV
	T_{MIN} to T_{MAX} variation		±4		µV/°C
Input Bias Current		−18	−13		µA
	T_{MIN} to T_{MAX} variation		−0.01		µA/°C
Input Resistance	Differential		6		MΩ
	Common mode		3		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage			$-V_S$ + 0.3 to $+V_S$ − 1.6		V
CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$; $\Delta V_{IN, cm}$ = ±1 V, f = 1 MHz		−75		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Maximum ΔV_{OUT}; single-ended output		$-V_S$ + 1.2 to $+V_S$ − 1.2		V
Linear Output Current	Per amplifier		95		mA
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$; $\Delta V_{OUT, dm}$ = 1 V; f = 10 MHz		−60		dB

Table 2. V_{OCM} to ±OUT Performance

Parameter	Conditions	Min	Typ	Max	Unit
V_{OCM} DYNAMIC PERFORMANCE					
−3 dB Bandwidth			230		MHz
Slew Rate	V_{IN} = −3.4 V to +3.4 V, 25% to 75%		1700		V/µs
Input Voltage Noise (RTI)			7.5		nV/√Hz
V_{OCM} INPUT CHARACTERISTICS					
Input Voltage Range			$-V_S$ + 1.3 to $+V_S$ − 1.3		V
Input Resistance			10		kΩ
Input Offset Voltage	$V_{OS, cm} = V_{OUT, cm}$; $V_{DIN+} = V_{DIN-}$ = 0 V		3		mV
Input Bias Current			0.5		µA
V_{OCM} CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V		−81		dB
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V	0.95	1.00	1.05	V/V
POWER SUPPLY					
Operating Range		4.5		11	V
Quiescent Current	Per amplifier		37	40	mA
	T_{MIN} to T_{MAX} variation		40		µA/°C
	Powered down		2.0	3.0	mA
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S$; ΔV_S = ±1 V		−80		dB
POWER DOWN ($\overline{PD}$)					
$\overline{PD}$ Input Voltage	Powered down		≤2.5		V
	Enabled		≥3		V
Turn-Off Time			1		µs
Turn-On Time			200		ns
$\overline{PD}$ Bias Current					
Enabled	$\overline{PD}$ = 5 V		1		µA
Disabled	$\overline{PD}$ = −5 V		−760		µA
OPERATING TEMPERATURE RANGE		−40		+85	°C

SINGLE-SUPPLY OPERATION

T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = 0 V, V_{OCM} = $+V_S$/2, R_T = 61.9 Ω, R_G = R_F = 200 Ω, G = +1, $R_{L, dm}$ = 1 kΩ, unless otherwise noted.
All specifications refer to single-ended input and differential output, unless otherwise noted. For gains other than G = 1, values for R_F and R_G are shown in Table 11.

Table 3. $\pm D_{IN}$ to ±OUT Performance

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	V_{OUT} = 0.1 V p-p		1000		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 2 V p-p		150		MHz
Large Signal Bandwidth	V_{OUT} = 2 V p-p		750		MHz
Slew Rate	V_{OUT} = 2 V p-p		3900		V/µs
Overdrive Recovery Time	V_{IN} = 2.5 V to 0 V step, G = +2		4		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	V_{OUT} = 2 V p-p, 10 MHz		−110		dBc
	V_{OUT} = 2 V p-p, 50 MHz		−79		dBc
Third Harmonic	V_{OUT} = 2 V p-p, 10 MHz		−100		dBc
	V_{OUT} = 2 V p-p, 50 MHz		−79		dBc
Input Voltage Noise	f = 10 MHz		2.6		nV/√Hz
Noise Figure	G = +4, f = 10 MHz		15.8		dB
Input Current Noise	f = 10 MHz		4.8		pA/√Hz
Crosstalk (ADA4938-2)	f = 100 MHz		−85		dB
INPUT CHARACTERISTICS					
Offset Voltage	$V_{OS, dm}$ = $V_{OUT, dm}$/2; V_{DIN+} = V_{DIN-} = V_{OCM} = 2.5 V		1	4	mV
	T_{MIN} to T_{MAX} variation		±4		µV/°C
Input Bias Current		−18	−13		µA
	T_{MIN} to T_{MAX} variation		−0.01		µA/°C
Input Resistance	Differential		6		MΩ
	Common mode		3		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage			$-V_S$ + 0.3 to $+V_S$ − 1.6		V
CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$; $\Delta V_{IN, cm}$ = ±1 V		−80		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Maximum ΔV_{OUT}; single-ended output		$-V_S$ + 1.2 to $+V_S$ − 1.2		V
Linear Output Current	Per amplifier		95		mA
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$; $\Delta V_{OUT, dm}$ = 1 V		−60		dB

Table 4. V_{OCM} to ±OUT Performance

Parameter	Conditions	Min	Typ	Max	Unit
V_{OCM} DYNAMIC PERFORMANCE					
−3 dB Bandwidth			400		MHz
Slew Rate	V_{IN} = 1.6 V to 3.4 V, 25% to 75%		1700		V/µs
Input Voltage Noise (RTI)			7.5		nV/√Hz
V_{OCM} INPUT CHARACTERISTICS					
Input Voltage Range			$-V_S$ + 1.3 to $+V_S$ − 1.3		V
Input Resistance			10		kΩ
Input Offset Voltage	$V_{OS, cm} = V_{OUT, cm}$; $V_{DIN+} = V_{DIN-} = V_{OCM}$ = 2.5 V		3		mV
Input Bias Current			0.5		µA
V_{OCM} CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V		−89		dB
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V	0.95	1.00	1.05	V/V
POWER SUPPLY					
Operating Range		4.5		11	V
Quiescent Current			34	36.5	mA
	T_{MIN} to T_{MAX} variation		40		µA/°C
	Powered down		1.0	1.7	mA
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S$; ΔV_S = ±1 V		−80		dB
POWER DOWN ($\overline{PD}$)					
$\overline{PD}$ Input Voltage	Powered down		≤2.5		V
	Enabled		≥3		V
Turn-Off Time			1		µs
Turn-On Time			200		ns
PD Bias Current					
Enabled	$\overline{PD}$ = 5 V		1		µA
Disabled	$\overline{PD}$ = 0 V		−260		µA
OPERATING TEMPERATURE RANGE		−40		+85	°C

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	12 V
Power Dissipation	See Figure 4
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device (including exposed pad) soldered to a high thermal conductivity 4-layer circuit board, as described in EIA/JESD 51-7. The exposed pad is not electrically connected to the device. It is typically soldered to a pad on the PCB that is thermally and electrically connected to an internal ground plane.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead LFCSP (Exposed Pad)	95	°C/W
24-Lead LFCSP (Exposed Pad)	65	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the ADA4938 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4938. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to the load drive depends upon the particular application. The power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, which effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads/exposed pad from metal traces, through-holes, ground, and power planes reduces the θ_{JA}.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 16-lead LFCSP (95°C/W) and the 24-lead LFCSP (65°C/W) on a JEDEC standard 4-layer board.

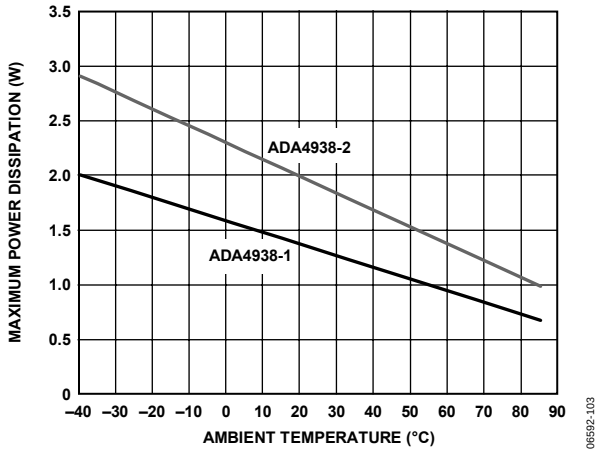

Figure 4. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

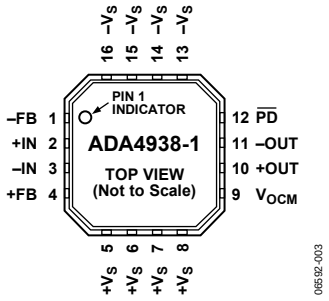

Figure 5. ADA4938-1 Pin Configuration

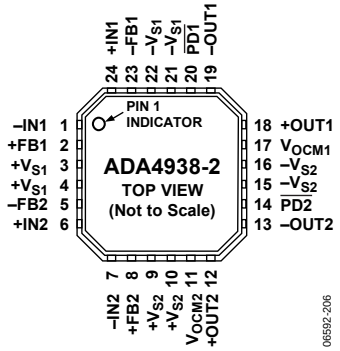

Figure 6. ADA4938-2 Pin Configuration

Table 7. ADA4938-1 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−FB	Negative Output Feedback Pin.
2	+IN	Positive Input Summing Node.
3	−IN	Negative Input Summing Node.
4	+FB	Positive Output Feedback Pin.
5 to 8	$+V_S$	Positive Supply Voltage.
9	V_{OCM}	Output Common-Mode Voltage.
10	+OUT	Positive Output for Load Connection.
11	−OUT	Negative Output for Load Connection.
12	$\overline{PD}$	Power-Down Pin.
13 to 16	$-V_S$	Negative Supply Voltage.

Table 8. ADA4938-2 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−IN1	Negative Input Summing Node 1.
2	+FB1	Positive Output Feedback Pin 1.
3, 4	$+V_{S1}$	Positive Supply Voltage 1.
5	−FB2	Negative Output Feedback Pin 2.
6	+IN2	Positive Input Summing Node 2.
7	−IN2	Negative Input Summing Node 2.
8	+FB2	Positive Output Feedback Pin 2.
9, 10	$+V_{S2}$	Positive Supply Voltage 2.
11	V_{OCM2}	Output Common-Mode Voltage 2.
12	+OUT2	Positive Output 2.
13	−OUT2	Negative Output 2.
14	$\overline{PD2}$	Power-Down Pin 2.
15, 16	$-V_{S2}$	Negative Supply Voltage 2.
17	V_{OCM1}	Output Common-Mode Voltage 1.
18	+OUT1	Positive Output 1.
19	−OUT1	Negative Output 1.
20	$\overline{PD1}$	Power-Down Pin 1.
21, 22	$-V_{S1}$	Negative Supply Voltage 1.
23	−FB1	Negative Output Feedback Pin 1.
24	+IN1	Positive Input Summing Node 1.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = −5 V, V_{OCM} = 0 V, R_T = 61.9 Ω, R_G = R_F = 200 Ω, G = +1, $R_{L, dm}$ = 1 kΩ, unless otherwise noted.
All measurements were performed with single-ended input and differential output, unless otherwise noted. For gains other than G = +1, values for R_F and R_G are shown in Table 11.

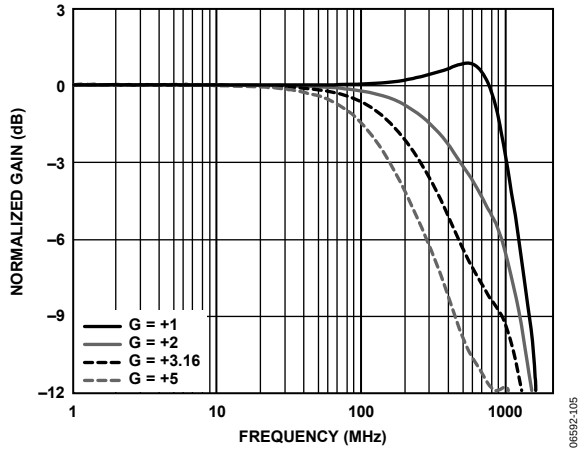

Figure 7. Small Signal Frequency Response for Various Gains, V_{OUT} = 0.1 V p-p

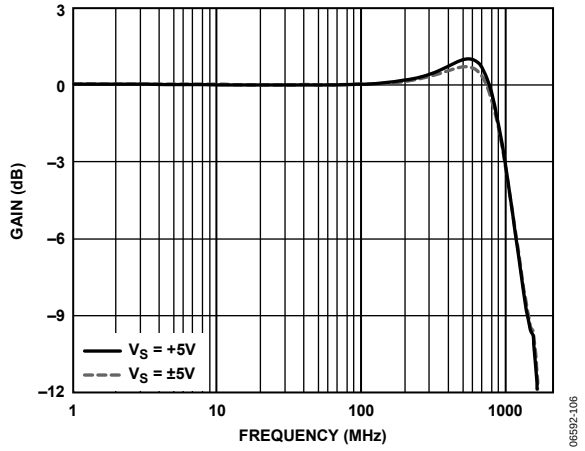

Figure 8. Small Signal Response for Various Supplies, V_{OUT} = 0.1 V p-p

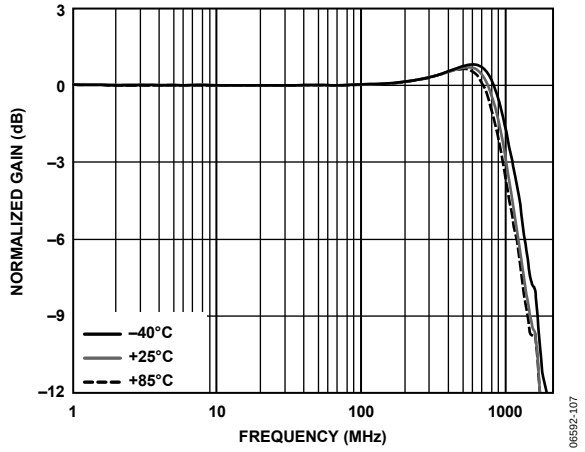

Figure 9. Small Signal Frequency Response for Various Temperatures, V_{OUT} = 0.1 V p-p

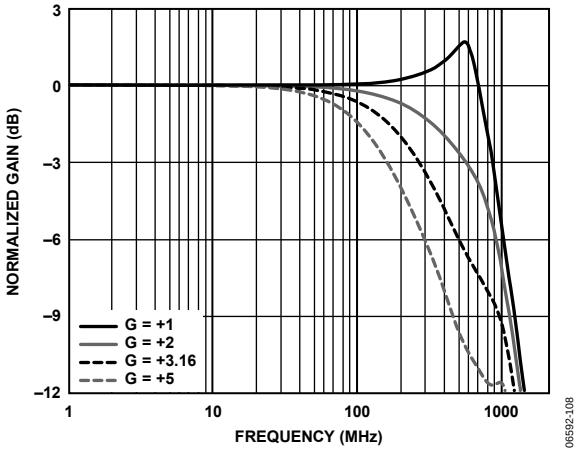

Figure 10. Large Signal Frequency Response for Various Gains

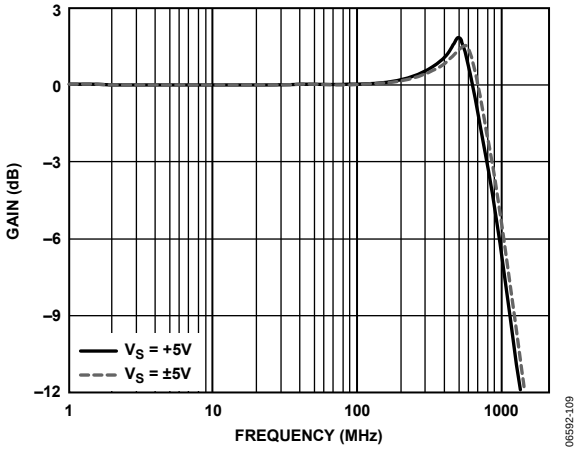

Figure 11. Large Signal Response for Various Supplies

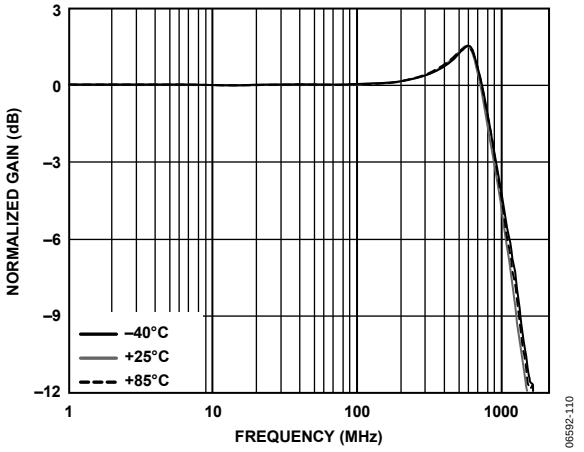

Figure 12. Large Signal Frequency Response for Various Temperatures

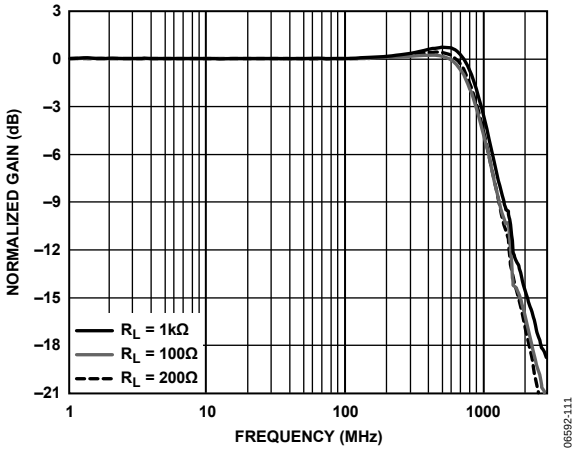

Figure 13. Small Signal Frequency Response for Various Loads, V_{OUT} = 0.1 V p-p

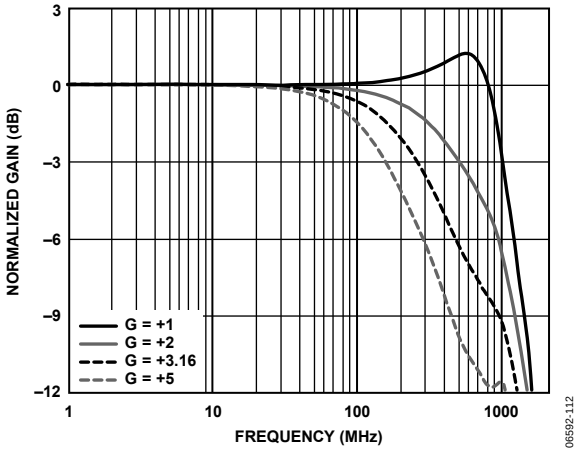

Figure 14. Small Signal Frequency Response for Various Gains, V_S = 5 V, V_{OUT} = 0.1 V p-p

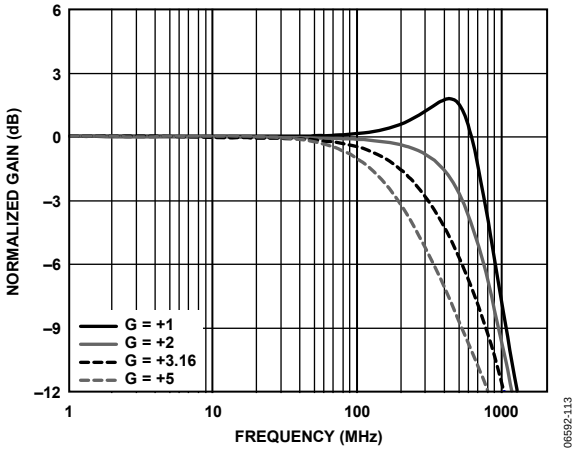

Figure 15. Small Signal Response for Various Gains, R_F = 402 Ω, V_{OUT} = 0.1 V p-p

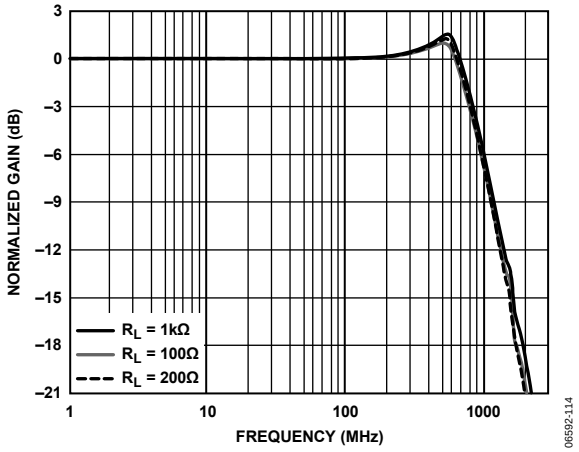

Figure 16. Large Signal Frequency Response for Various Loads

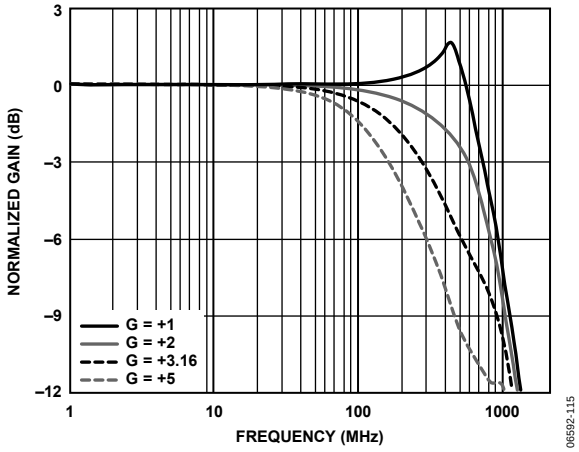

Figure 17. Large Signal Frequency Response for Various Gains, V_S = 5 V

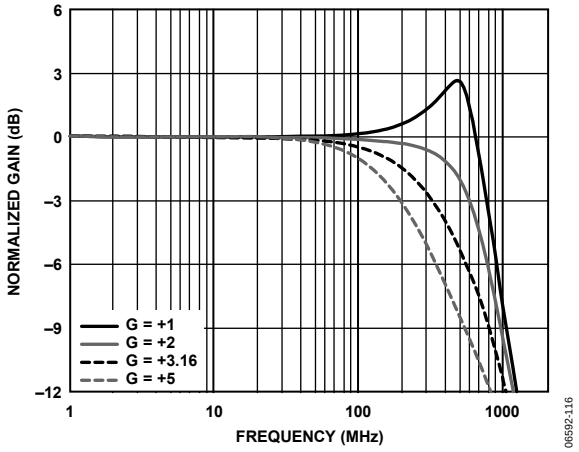

Figure 18. Large Signal Response for Various Gains, R_F = 402 Ω

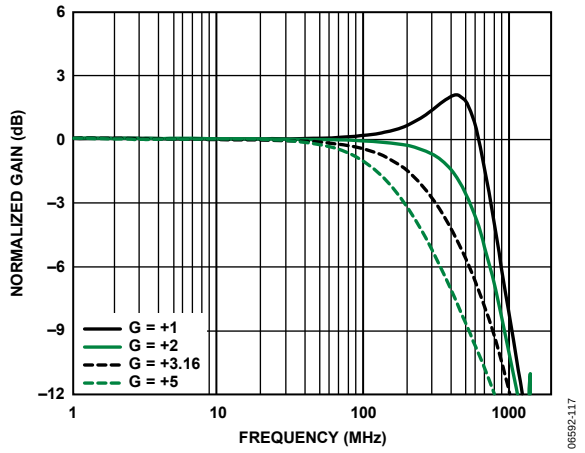

Figure 19. Small Signal Frequency Response for Various Gains, R_F = 402 Ω, V_S = 5 V, V_{OUT} = 0.1 V p-p

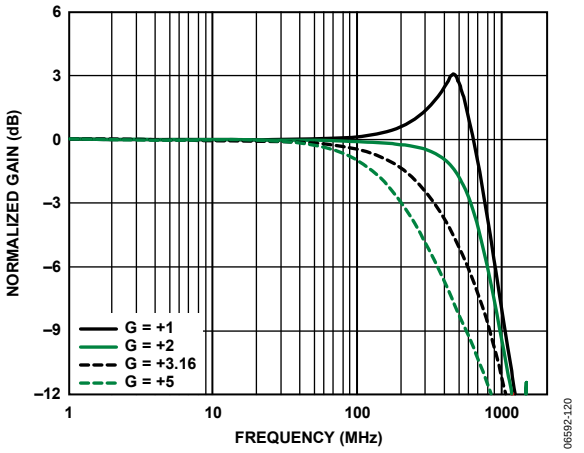

Figure 22. Large Signal Frequency Response for Various Gains, R_F = 402 Ω, V_S = 5 V

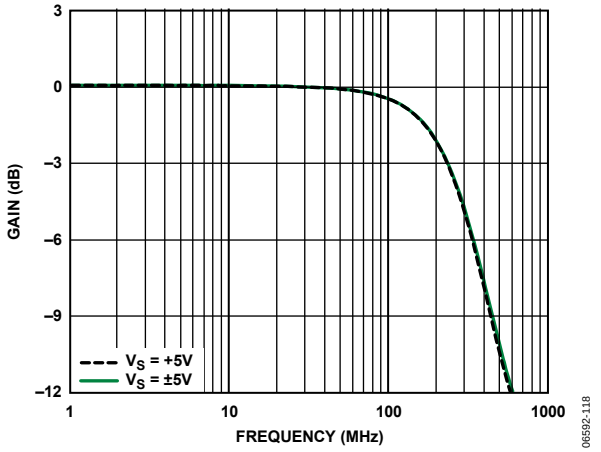

Figure 20. $V_{OUT, cm}$ Small Signal Frequency Response, V_{OUT} = 0.1 V p-p

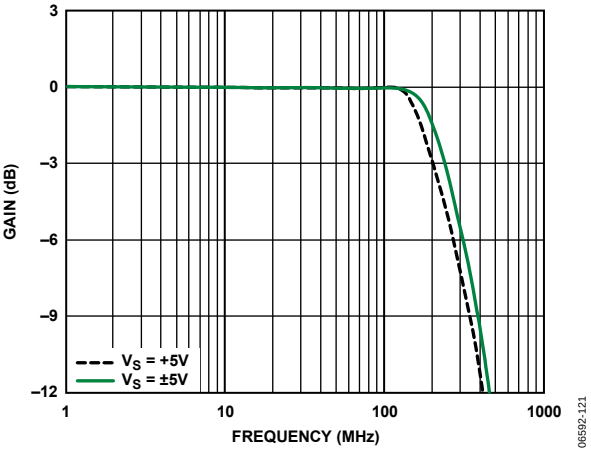

Figure 23. $V_{OUT, cm}$ Large Signal Frequency Response

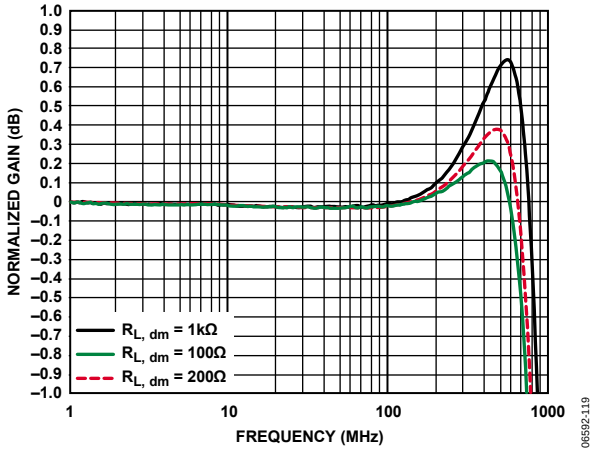

Figure 21. 0.1 dB Flatness Response for Various Loads, ADA4938-1, V_{OUT} = 0.1 V p-p

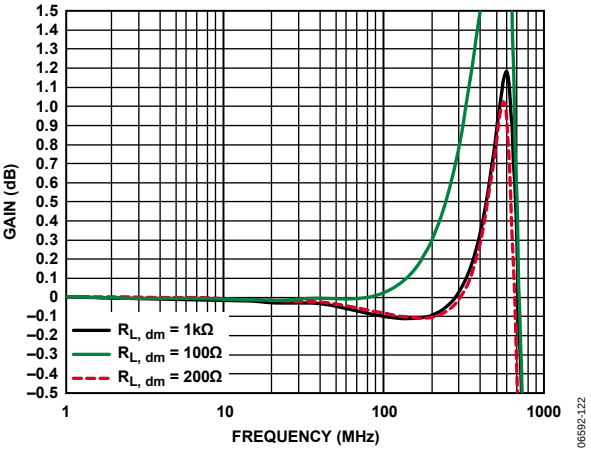

Figure 24. 0.1 dB Flatness Response for Various Loads, ADA4938-2, V_{OUT} = 0.1 V p-p

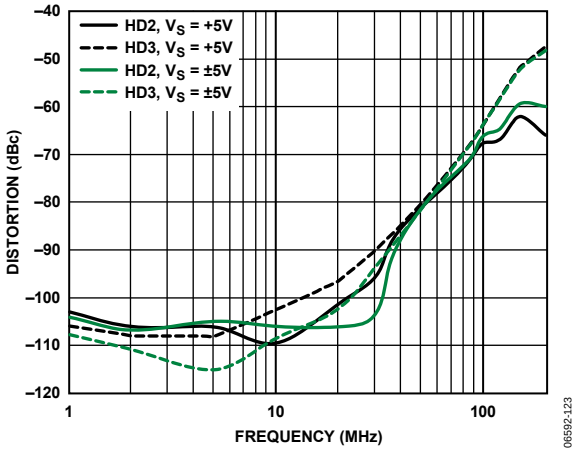

Figure 25. Harmonic Distortion vs. Frequency and Supply Voltage

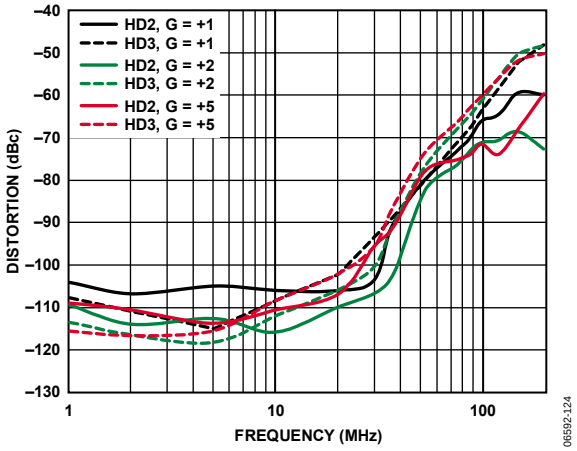

Figure 26. Harmonic Distortion vs. Frequency and Gain

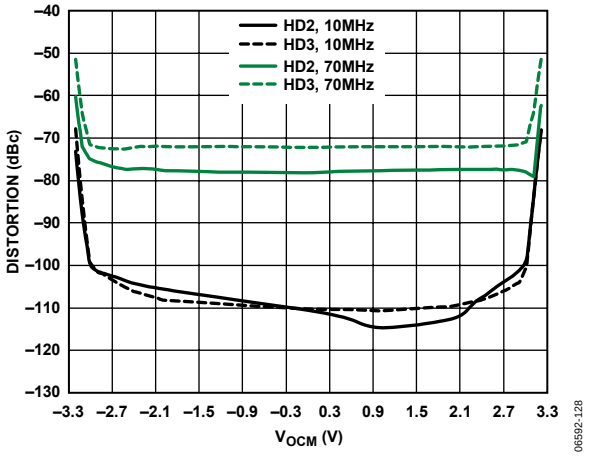

Figure 27. Harmonic Distortion vs. V_{OCM} and Frequency

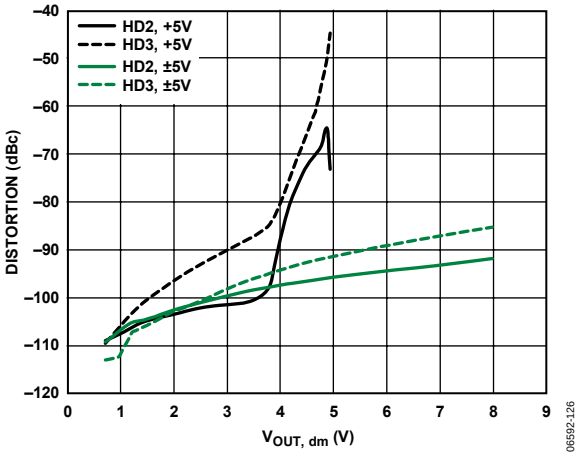

Figure 28. Harmonic Distortion vs. V_{OUT} and Supply Voltage

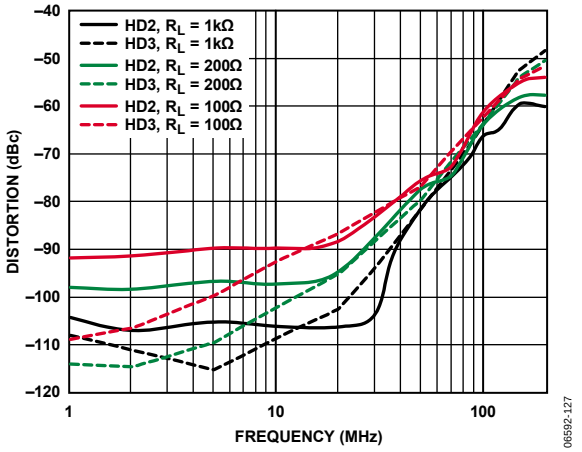

Figure 29. Harmonic Distortion vs. Frequency for Various Loads

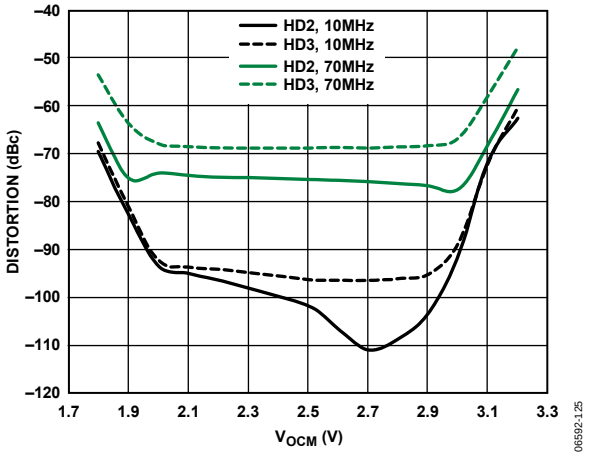

Figure 30. Harmonic Distortion vs. V_{OCM} and Frequency, V_S = 5 V

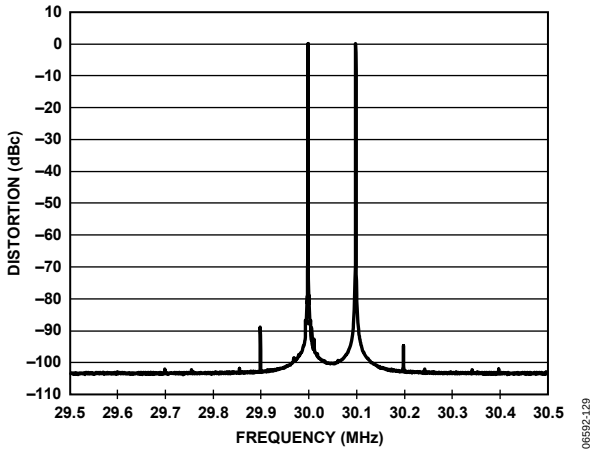

Figure 31. Intermodulation Distortion

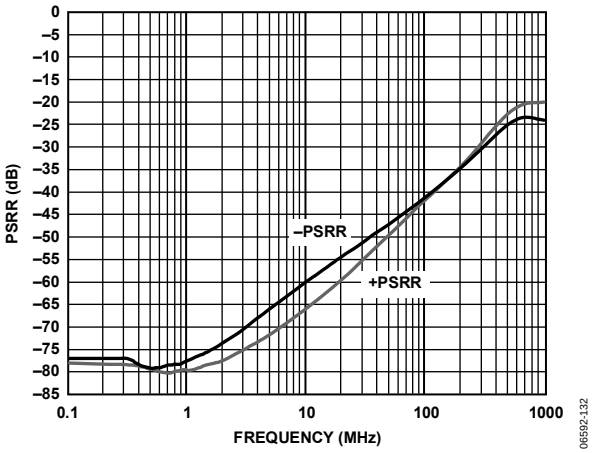

Figure 34. PSRR vs. Frequency

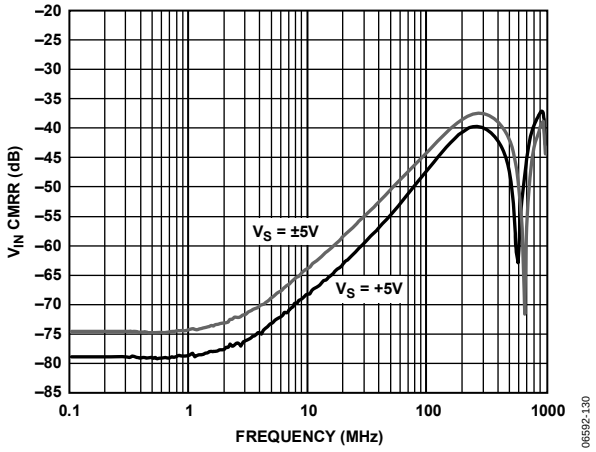

Figure 32. V_{IN} CMRR vs. Frequency

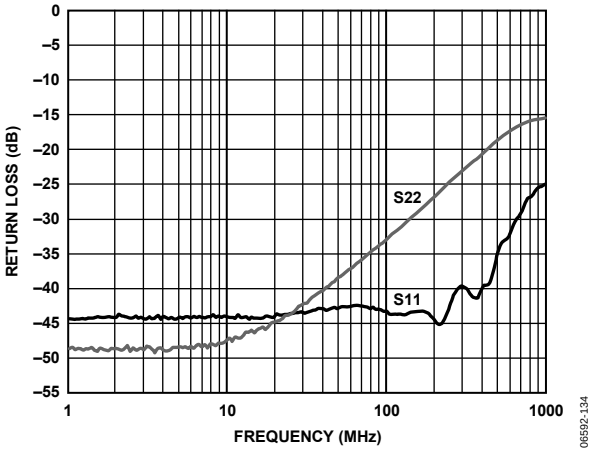

Figure 35. Return Loss (S11, S22) vs. Frequency

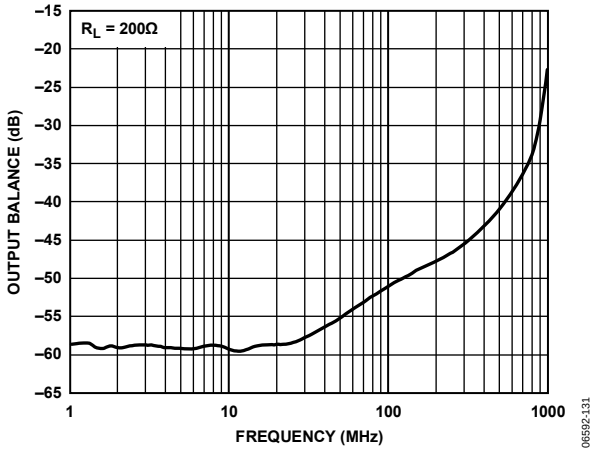

Figure 33. Output Balance vs. Frequency

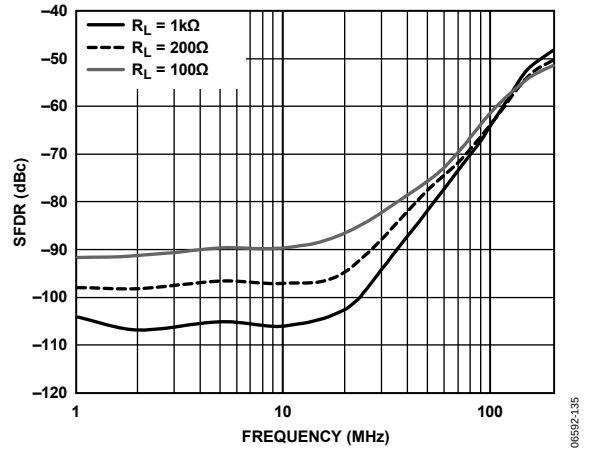

Figure 36. SFDR vs. Frequency for Various Loads

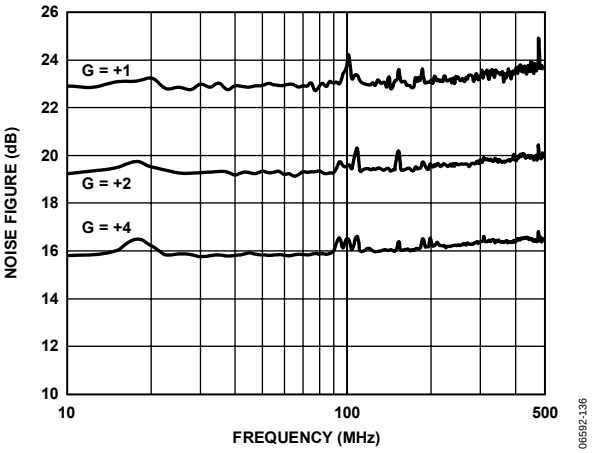

Figure 37. Noise Figure vs. Frequency

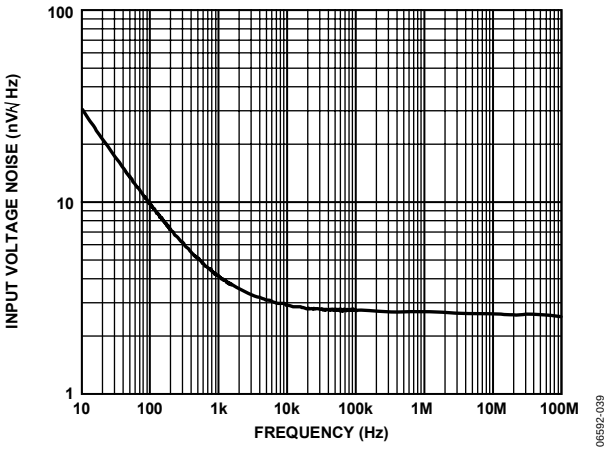

Figure 40. Input Voltage Noise vs. Frequency

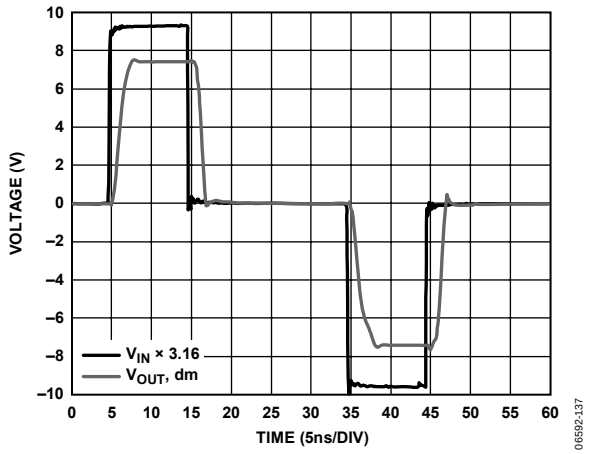

Figure 38. Overdrive Recovery Time (Pulse Input)

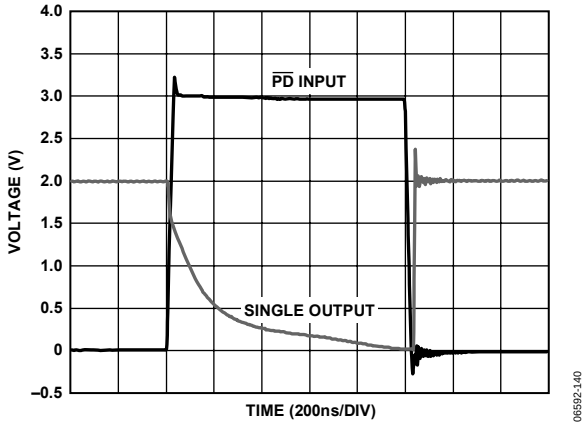

Figure 41. Power-Down Response Time

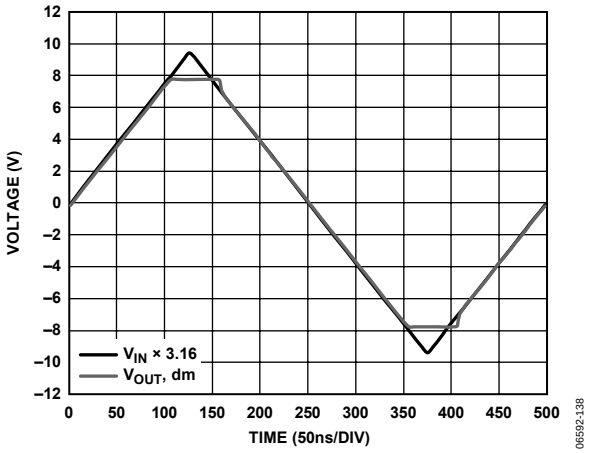

Figure 39. Overdrive Amplitude Characteristics (Triangle Wave Input)

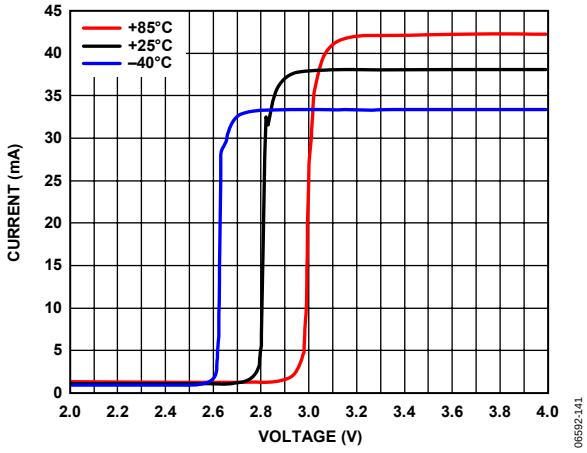

Figure 42. Supply Current vs. Power-Down Voltage and Temperature

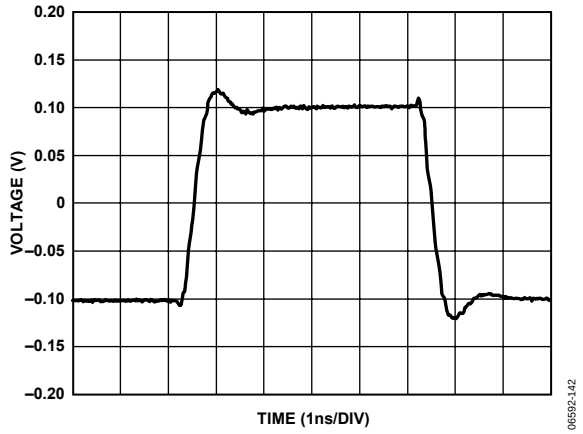

Figure 43. Small Signal Transient Response, V_{OUT} = 0.1 V p-p

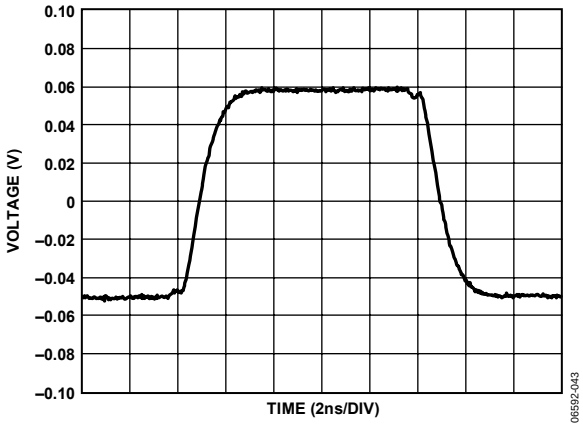

Figure 44. V_{OCM} Small Signal Transient Response, V_{OUT} = 0.1 V p-p

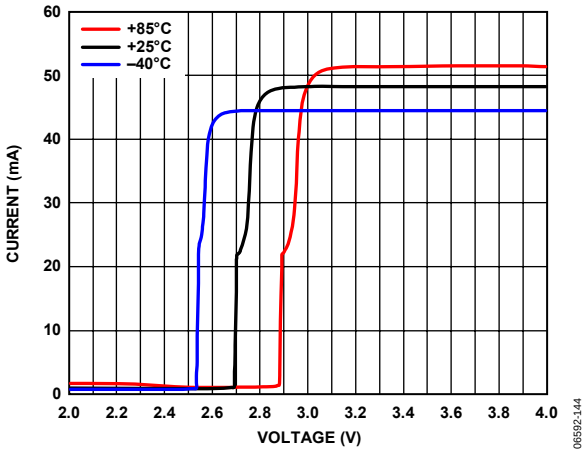

Figure 45. Supply Current vs. Power-Down Voltage and Temperature, V_S = 5 V

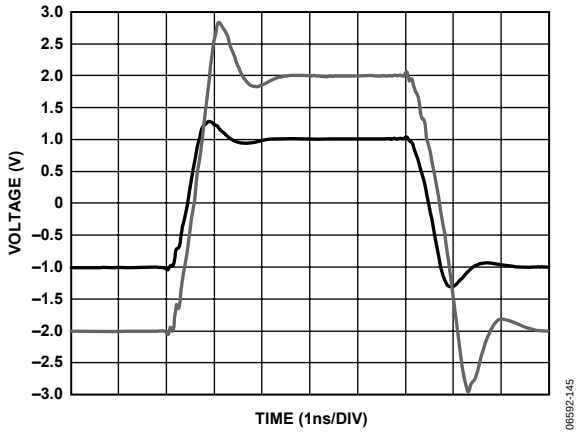

Figure 46. Large Signal Transient Response

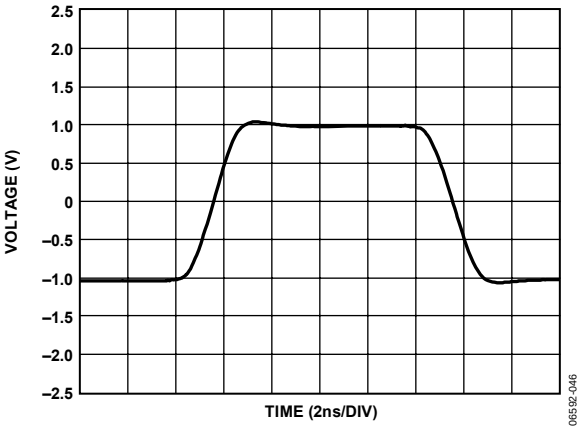

Figure 47. V_{OCM} Large Signal Transient Response

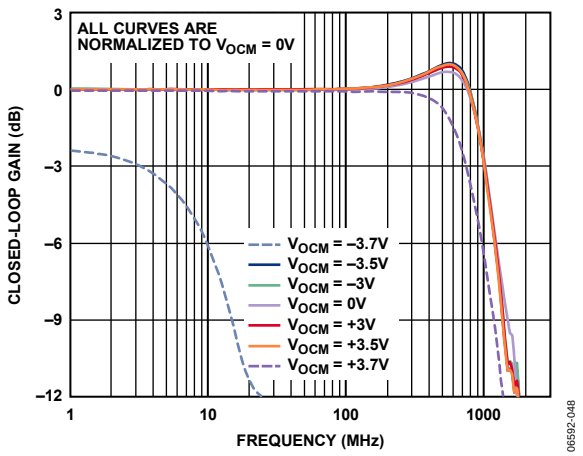

Figure 48. $V_{OUT, dm}$ Small Signal Frequency Response for Various V_{OCM}, V_{OUT} = 0.1 V p-p

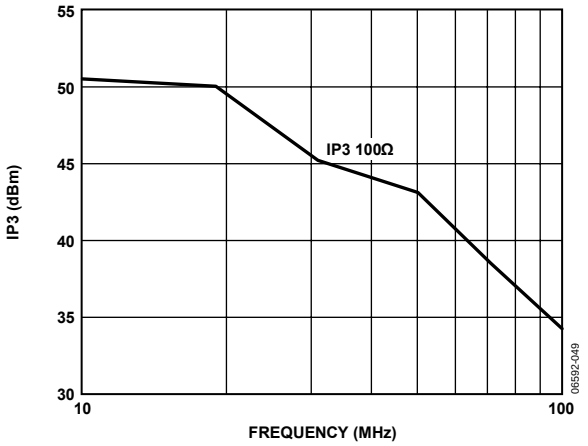

Figure 49. IP3 vs. Frequency

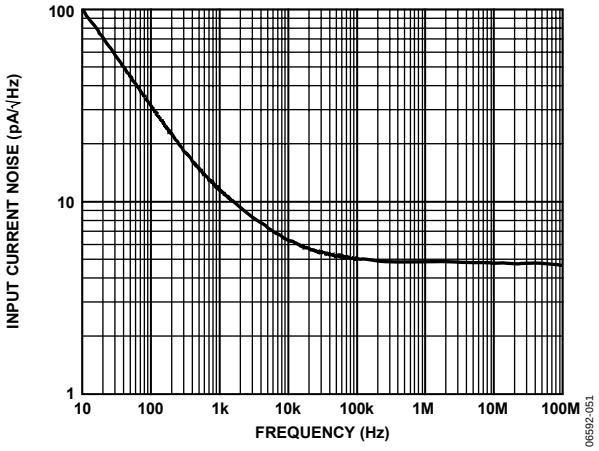

Figure 51. Input Current Noise vs. Frequency

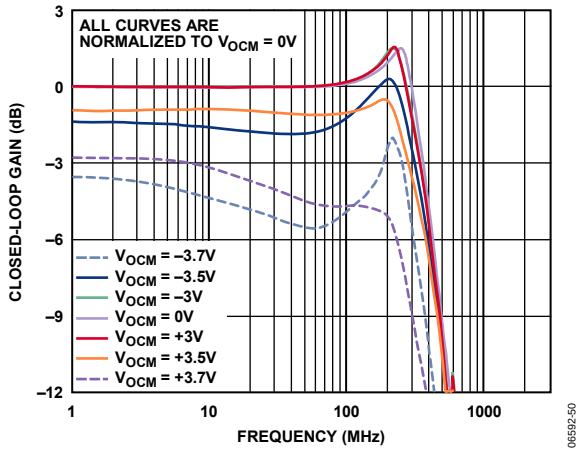

Figure 50. $V_{OUT, dm}$ Large Signal Frequency Response for Various V_{OCM}

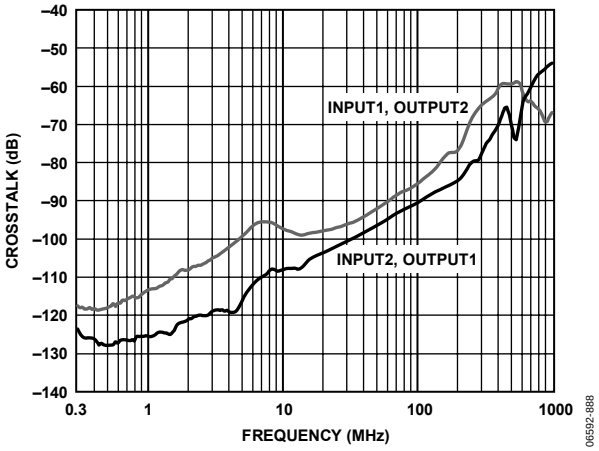

Figure 52. Crosstalk vs. Frequency for ADA4938-2

TEST CIRCUTS

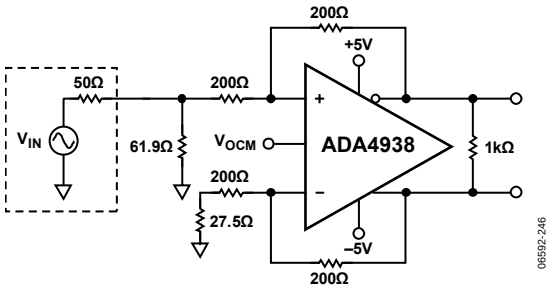

Figure 53. Equivalent Basic Test Circuit

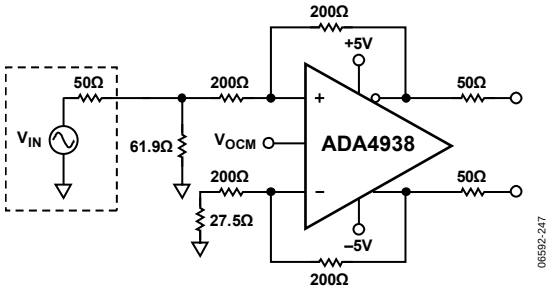

Figure 54. Test Circuit for Output Balance

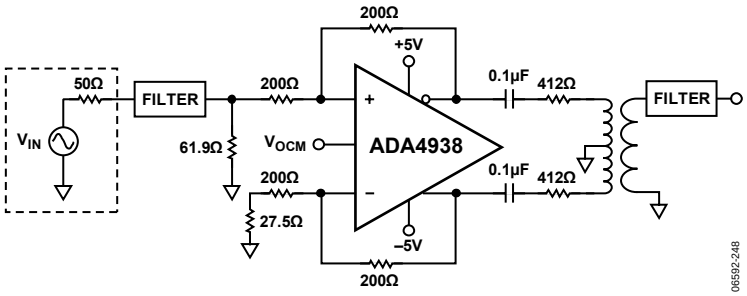

Figure 55. Test Circuit for Distortion Measurements

OPERATIONAL DESCRIPTION

DEFINITION OF TERMS

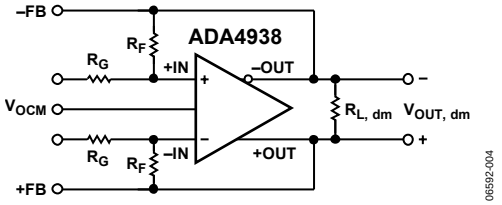

Figure 56. Circuit Definitions

Differential Voltage

The differential voltage is the difference between two node voltages. For example, the output differential voltage (or equivalently, output differential-mode voltage) is defined as

$$V_{OUT,\,dm} = (V_{+OUT} - V_{-OUT})$$

where V_{+OUT} and V_{-OUT} refer to the voltages at the +OUT and −OUT terminals with respect to a common reference.

Common-Mode Voltage

The common-mode voltage is the average of two node voltages. The output common-mode voltage is defined as

$$V_{OUT,\,cm} = (V_{+OUT} + V_{-OUT})/2$$

Balance

Balance is a measure of how well differential signals are matched in amplitude and are exactly 180° apart in phase. Balance is most easily determined by placing a well-matched resistor divider between the differential voltage nodes and comparing the magnitude of the signal at the midpoint of the divider with the magnitude of the differential signal. By this definition, output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential mode voltage.

$$Output\ Balance\ Error = \left| \frac{V_{OUT,\,cm}}{V_{OUT,\,dm}} \right|$$

THEORY OF OPERATION

The ADA4938 differs from conventional op amps in that it has two outputs whose voltages move in opposite directions. Like an op amp, it relies on open-loop gain and negative feedback to force these outputs to the desired voltages. The ADA4938 behaves much like a standard voltage feedback op amp and makes it easier to perform single-ended-to-differential conversions, common-mode level shifting, and amplifications of differential signals. Also like an op amp, the ADA4938 has high input impedance and low output impedance.

Two feedback loops are employed to control the differential and common-mode output voltages. The differential feedback, set with external resistors, controls only the differential output voltage. The common-mode feedback controls only the common-mode output voltage. This architecture makes it easy to set the output common-mode level to any arbitrary value. It is forced, by internal common-mode feedback, to be equal to the voltage applied to the V_{OCM} input, without affecting the differential output voltage.

The ADA4938 architecture results in outputs that are highly balanced over a wide frequency range without requiring tightly matched external components. The common-mode feedback loop forces the signal component of the output common-mode voltage to zero, which results in nearly perfectly balanced differential outputs that are identical in amplitude and are exactly 180° apart in phase.

ANALYZING AN APPLICATION CIRCUIT

The ADA4938 uses open-loop gain and negative feedback to force its differential and common-mode output voltages in such a way as to minimize the differential and common-mode error voltages. The differential error voltage is defined as the voltage between the differential inputs labeled +IN and −IN (see Figure 56). For most purposes, this voltage can be assumed to be zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to V_{OCM} can also be assumed to be zero. Starting from these two assumptions, any application circuit can be analyzed.

SETTING THE CLOSED-LOOP GAIN

The differential-mode gain of the circuit in Figure 56 can be determined by

$$\left|\frac{V_{OUT,dm}}{V_{IN,dm}}\right| = \frac{R_F}{R_G}$$

This assumes the input resistors (R_G) and feedback resistors (R_F) on each side are equal.

ESTIMATING THE OUTPUT NOISE VOLTAGE

The differential output noise of the ADA4938 can be estimated using the noise model in Figure 57. The input-referred noise voltage density, v_{nIN}, is modeled as a differential input, and the noise currents, i_{nIN-} and i_{nIN+}, appear between each input and ground. The noise currents are assumed to be equal and produce a voltage across the parallel combination of the gain and feedback resistances. v_{nCM} is the noise voltage density at the V_{OCM} pin. Each of the four resistors contributes $(4kTR)^{1/2}$. Table 9 summarizes the input noise sources, the multiplication factors, and the output-referred noise density terms.

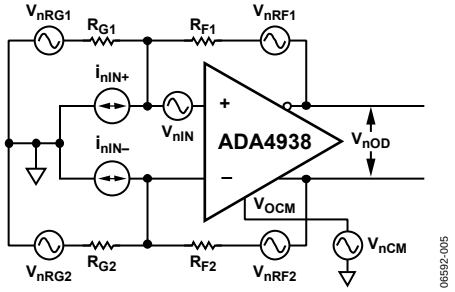

Figure 57. ADA4938 Noise Model

Table 9. Output Noise Voltage Density Calculations

Input Noise Contribution	Input Noise Term	Input Noise Voltage Density	Output Multiplication Factor	Output Noise Voltage Density Term
Differential Input	v_{nIN}	v_{nIN}	G_N	$v_{nO1} = G_N(v_{nIN})$
Inverting Input	i_{nIN-}	$i_{nIN-} \times (R_{G2}\|\|R_{F2})$	G_N	$v_{nO2} = G_N[i_{nIN-} \times (R_{G2}\|\|R_{F2})]$
Noninverting Input	i_{nIN+}	$i_{nIN+} \times (R_{G1}\|\|R_{F1})$	G_N	$v_{nO3} = G_N[i_{nIN+} \times (R_{G1}\|\|R_{F1})]$
V_{OCM} Input	v_{nCM}	v_{nCM}	$G_N(\beta_1 - \beta_2)$	$v_{nO4} = G_N(\beta_1 - \beta_2)(v_{nCM})$
Gain Resistor, R_{G1}	v_{nRG1}	$(4kTR_{G1})^{1/2}$	$G_N(1 - \beta_2)$	$v_{nO5} = G_N(1 - \beta_2)(4kTR_{G1})^{1/2}$
Gain Resistor, R_{G2}	v_{nRG2}	$(4kTR_{G2})^{1/2}$	$G_N(1 - \beta_1)$	$v_{nO6} = G_N(1 - \beta_1)(4kTR_{G2})^{1/2}$
Feedback Resistor, R_{F1}	v_{nRF1}	$(4kTR_{F1})^{1/2}$	1	$v_{nO7} = (4kTR_{F1})^{1/2}$
Feedback Resistor, R_{F2}	v_{nRF2}	$(4kTR_{F2})^{1/2}$	1	$v_{nO8} = (4kTR_{F2})^{1/2}$

Similar to the case of a conventional op amp, the output noise voltage densities can be estimated by multiplying the input-referred terms at +IN and −IN by the appropriate output factor, where:

$G_N = \frac{2}{(\beta_1 + \beta_2)}$ is the circuit noise gain.

$\beta_1 = \frac{R_{G1}}{R_{F1} + R_{G1}}$ and $\beta_2 = \frac{R_{G2}}{R_{F2} + R_{G2}}$ are the feedback factors.

When $R_{F1}/R_{G1} = R_{F2}/R_{G2}$, $\beta 1 = \beta 2 = \beta$, and the noise gain becomes

$$G_N = \frac{1}{\beta} = 1 + \frac{R_F}{R_G}$$

Note that the output noise from V_{OCM} goes to zero in this case. The total differential output noise density, v_{nOD}, is the root-sum-square of the individual output noise terms.

$$v_{nOD} = \sqrt{\sum_{i=1}^{8} v_{nOi}^2}$$

THE IMPACT OF MISMATCHES IN THE FEEDBACK NETWORKS

As previously mentioned, even if the external feedback networks (R_F/R_G) are mismatched, the internal common-mode feedback loop still forces the outputs to remain balanced. The amplitudes of the signals at each output remain equal and 180° out of phase. The input-to-output, differential mode gain varies proportionately to the feedback mismatch, but the output balance is unaffected.

As well as causing a noise contribution from V_{OCM}, ratio matching errors in the external resistors result in a degradation of the ability of the circuit to reject input common-mode signals, much the same as for a four-resistor difference amplifier made from a conventional op amp.

In addition, if the dc levels of the input and output common-mode voltages are different, matching errors result in a small differential-mode output offset voltage. When G = +1, with a ground referenced input signal and the output common-mode level set to 2.5 V, an output offset of as much as 25 mV (1% of the difference in common-mode levels) can result if 1% tolerance resistors are used. Resistors of 1% tolerance result in a worst-case input CMRR of about 40 dB, a worst-case differential-mode output offset of 25 mV due to 2.5 V level-shift, and no significant degradation in output balance error.

CALCULATING THE INPUT IMPEDANCE OF AN APPLICATION CIRCUIT

The effective input impedance of a circuit depends on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, as shown in Figure 58, the input impedance ($R_{IN, dm}$) between the inputs ($+D_{IN}$ and $-D_{IN}$) is simply $R_{IN, dm} = 2 \times R_G$.

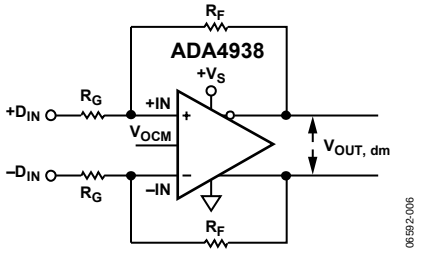

Figure 58. ADA4938 Configured for Balanced (Differential) Inputs

For an unbalanced, single-ended input signal (see Figure 59), the input impedance is

$$R_{IN,cm} = \left(\frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right)$$

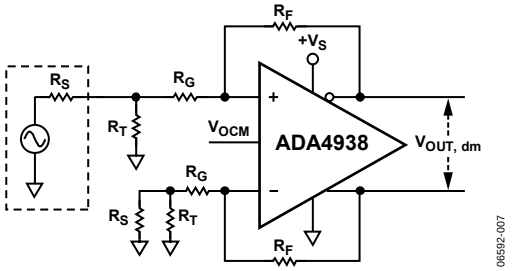

Figure 59. ADA4938 Configured for Unbalanced (Single-Ended) Input

The input impedance of the circuit is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor R_G.

INPUT COMMON-MODE VOLTAGE RANGE IN SINGLE-SUPPLY APPLICATIONS

The ADA4938 is optimized for level-shifting, ground-referenced input signals. As such, the center of the input common-mode range is shifted approximately 1 V down from midsupply. The input common-mode range at the summing nodes of the amplifier is from 0.3 V above $-V_S$ to 1.6 V below $+V_S$. To avoid clipping at the outputs, the voltage swing at the +IN and −IN terminals must be confined to these ranges.

TERMINATING A SINGLE-ENDED INPUT

Using an example with an input source of 2 V, a source resistance of 50 Ω, and an overall gain of 1 V/V, four simple steps must be followed to terminate a single-ended input to the ADA4938.

1. The input impedance is calculated using the formula

$$R_{IN} = \left(\frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right) = \left(\frac{200}{1 - \frac{200}{2 \times (200 + 200)}} \right) = 267\ \Omega$$

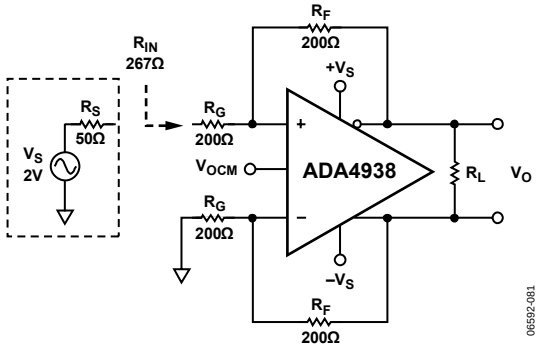

Figure 60. Single-Ended Input Impedance

2. To provide a 50 Ω termination for the source, the Resistor R_T is calculated such that $R_T \parallel R_{IN} = 50\ \Omega$, or $R_T = 61.9\ \Omega$.

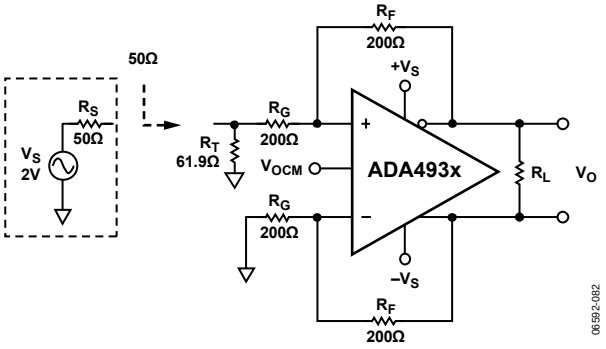

Figure 61. Adding Termination Resistor R_T

3. To compensate for the imbalance of the gain resistors, a correction resistor (R_{TS}) is added in series with the inverting input gain resistor R_G. R_{TS} is equal to the Thevenin equivalent of the source resistance $R_S \parallel R_T$.

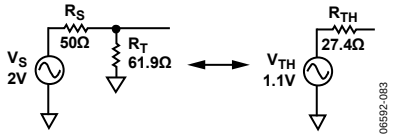

Figure 62. Calculating Thevenin Equivalent

$R_{TS} = R_{TH} = R_S \parallel R_T = 27.4\ \Omega$. Note that V_{TH} is not equal to $V_S/2$, which would be the case if the amplifier circuit did not affect the termination.

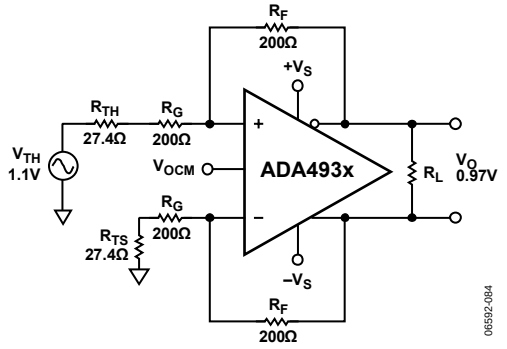

Figure 63. Balancing Gain Resistor R_G

4. Finally, the feedback resistor is recalculated to adjust the output voltage to the desired level.

   a. To make the output voltage $V_O = 1$ V, R_F is calculated using

$$R_F = \left(\frac{V_O \times (R_G + R_{TS})}{V_{TH}} \right) = \left(\frac{1 \times (200 + 27.4)}{1.1} \right) = 207\ \Omega$$

   b. To get the overall gain back to 1 V/V ($V_O = V_S = 2$ V), R_F should be

$$R_F = \left(\frac{V_O \times (R_G + R_{TS})}{V_{TH}} \right) = \left(\frac{2 \times (200 + 27.4)}{1.1} \right) = 414\ \Omega$$

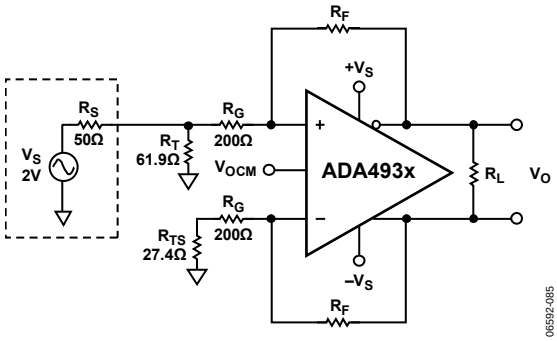

Figure 64. Complete Single-Ended-to-Differential System

SETTING THE OUTPUT COMMON-MODE VOLTAGE

The V_{OCM} pin of the ADA4938 is internally biased at a voltage approximately equal to the midsupply point (average value of the voltages on V+ and V−). Relying on this internal bias results in an output common-mode voltage that is within about 100 mV of the expected value.

In cases where more accurate control of the output common-mode level is required, it is recommended that an external source, or resistor divider (10 kΩ or greater resistors), be used.

It is also possible to connect the V_{OCM} input to a common-mode level (CML) output of an ADC. However, care must be taken to assure that the output has sufficient drive capability. The input impedance of the V_{OCM} pin is approximately 10 kΩ. If multiple ADA4938 devices share one reference output, it is recommended that a buffer be used.

Table 10 and Table 11 list several common gain settings, associated resistor values, input impedances, and output noise densities for both balanced and unbalanced input configurations. Also shown are the input common-mode voltages under the given conditions for different V_{OCM} settings for both a 10 V single supply and ±5 V dual supplies.

Table 10. Differential Ground-Referenced Input, DC-Coupled; See Figure 58

Nominal Gain (V/V)	R_F (Ω)	R_G (Ω)	$R_{IN, dm}$ (Ω)	Differential Output Noise Density (nV/√Hz)	Common-Mode Level at +IN, −IN (V)			
					$+V_S$ = 10 V, $-V_S$ = 0 V, $V_{OUT, dm}$ = 2.0 V p-p		$+V_S$ = 5 V, $-V_S$ = −5 V, $V_{OUT, dm}$ = 2.0 V p-p	
					V_{OCM} = 2.5 V	V_{OCM} = 3.5 V	V_{OCM} = 1.0 V	V_{OCM} = 3.2 V
1	200	200	400	6.5	1.25	1.75	0.50	1.60
2	402	200	400	10.4	0.83	1.16	0.33	1.06
3.16	402	127	254	13.4	0.60	0.84	0.24	0.77
5	402	80.6	161	18.2	0.42	0.58	0.17	0.53

Table 11. Single-Ended Ground-Referenced Input, DC-Coupled, R_S = 50 Ω; See Figure 59

Nominal Gain (V/V)	R_F (Ω)	R_{G1} (Ω)	R_T (Ω)	$R_{IN,se}$ (Ω)	R_{G2} (Ω)[1]	Overall Gain (V/V)[2]	Differential Output Noise Density (nV/√Hz)	Common-Mode Swing at +IN, −IN (V)			
								$+V_S$ = 10 V, $-V_S$ = 0 V, $V_{OUT, dm}$ = 2.0 V p-p		$+V_S$ = 5 V, $-V_S$ = −5 V, $V_{OUT, dm}$ = 2.0 V p-p	
								V_{OCM} = 2.5 V	V_{OCM} = 3.5 V	V_{OCM} = 0 V	V_{OCM} = 2.0 V
1	200	200	60.4	267	226	0.9	6.2	1.00 to 1.50	1.50 to 2.00	−0.25 to +0.25	0.75 to 1.25
2	402	200	60.4	300	226	1.8	9.8	0.66 to 1.00	1.00 to 1.33	−0.17 to +0.17	0.50 to 0.83
3.16	402	127	66.5	205	158	2.5	11.8	0.48 to 0.72	0.72 to 0.96	−0.12 to +0.12	0.36 to 0.60
5	402	80.6	76.8	138	110	3.6	14.7	0.33 to 0.50	0.50 to 0.67	−0.08 to +0.08	0.25 to 0.42

[1] $R_{G2} = R_{G1} + R_{TS}$.
[2] Includes effects of termination match.

LAYOUT, GROUNDING, AND BYPASSING

As a high speed device, the ADA4938 is sensitive to the PCB environment in which it operates. Realizing its superior performance requires attention to the details of high speed PCB design.

The first requirement is a solid ground plane that covers as much of the board area around the ADA4938 as possible. However, the area near the feedback resistors (R_F), gain resistors (R_G), and the input summing nodes should be cleared of all ground and power planes (see Figure 65). Clearing the ground and power planes minimizes any stray capacitance at these nodes and prevents peaking of the response of the amplifier at high frequencies.

The thermal resistance, θ_{JA}, is specified for the device, including the exposed pad, soldered to a high thermal conductivity 4-layer circuit board, as described in EIA/JESD 51-7. The exposed pad is electrically isolated from the device; therefore, it may be connected to a ground plane using vias. Examples of the thermal attach pad and via structure for the ADA4938-1 are shown in Figure 66 and Figure 67.

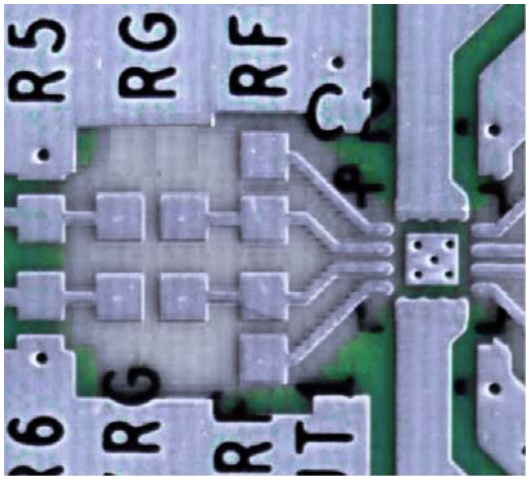

Figure 65. Ground and Power Plane Voiding in Vicinity of R_F and R_G

The power supply pins should be bypassed as close to the device as possible and directly to a nearby ground plane. High frequency ceramic chip capacitors should be used. It is recommended that two parallel bypass capacitors (1000 pF and 0.1 µF) be used for each supply. The 1000 pF capacitor should be placed closer to the device. Further away, low frequency bypassing should be provided, using 10 µF tantalum capacitors from each supply to ground.

Signal routing should be short and direct to avoid parasitic effects. Wherever complementary signals exist, a symmetrical layout should be provided to maximize balanced performance. When routing differential signals over a long distance, PCB traces should be close together, and any differential wiring should be twisted such that loop area is minimized. Doing this reduces radiated energy and makes the circuit less susceptible to interference.

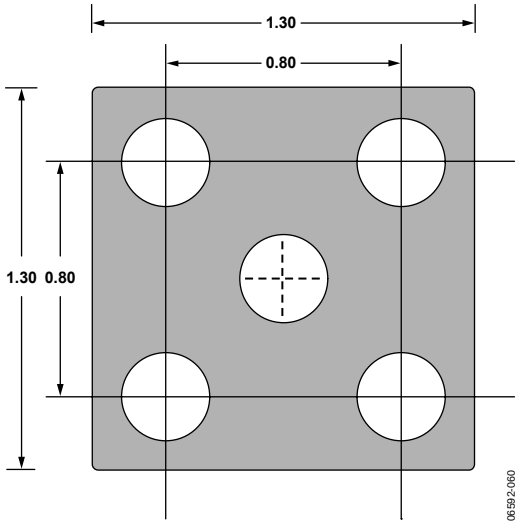

Figure 66. Recommended PCB Thermal Attach Pad (ADA4938-1) (Dimensions in Millimeters)

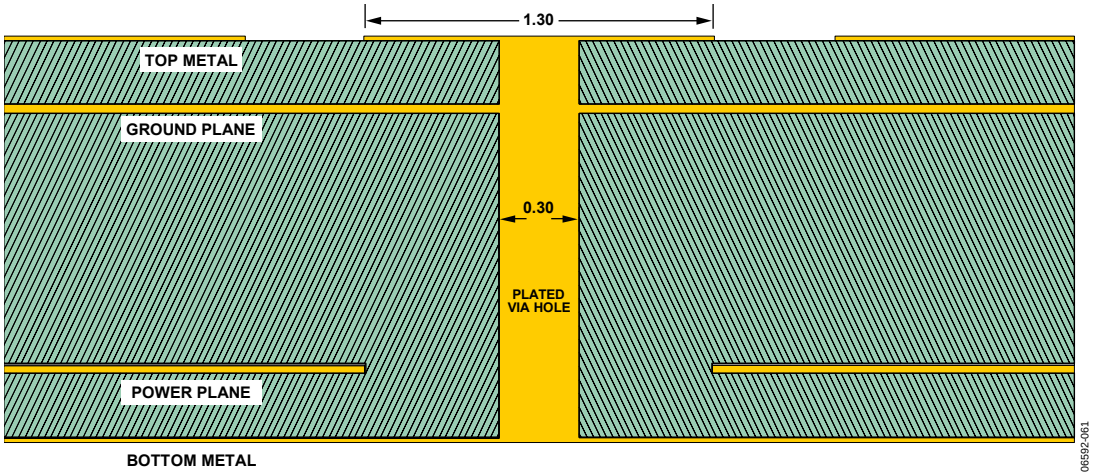

Figure 67. Cross-Section of a 4-Layer PCB (ADA4938-1) Showing a Thermal Via Connection to the Buried Ground Plane (Dimensions in Millimeters)

HIGH PERFORMANCE ADC DRIVING

The ADA4938 is ideally suited for dc-coupled baseband applications. The circuit in Figure 68 shows a front-end connection for an ADA4938 driving an AD9446, 16-bit, 80 MSPS ADC. The AD9446 achieves its optimum performance when it is driven differentially. The ADA4938 eliminates the need for a transformer to drive the ADC, performs a single-ended-to-differential conversion, buffers the driving signal, and provides appropriate level shifting for dc coupling.

The ADA4938 is configured with a single 10 V supply and unity gain for a single-ended input to differential output. The 61.9 Ω termination resistor, in parallel with the single-ended input impedance of 267 Ω, provides a 50 Ω termination for the source. The additional 26 Ω (226 Ω total) at the inverting input balances the parallel impedance of the 50 Ω source and the termination resistor driving the noninverting input.

The signal generator has a symmetric, ground-referenced bipolar output. The V_{OCM} pin of the ADA4938 is biased with an external resistor divider to obtain the desired 3.5 V output common-mode. One-half of the common-mode voltage is fed back to the summing nodes, biasing –IN and + IN at 1.75 V. For a common-mode voltage of 3.5 V, each ADA4938 output swings between 2.7 V and 4.3 V, providing a 3.2 V p-p differential output.

The output of the amplifier is dc-coupled to the ADC through a second-order, low-pass filter with a –3 dB frequency of 50 MHz. The filter reduces the noise bandwidth of the amplifier and isolates the driver outputs from the ADC inputs.

The AD9446 is configured for a 4.0 V p-p full-scale input by setting R1 = R2 = 1 kΩ between the VREF pin and SENSE pin in Figure 68.

The circuit in Figure 69 shows a simplified front-end connection for an ADA4938 driving an AD9246, 14-bit, 125 MSPS ADC. The AD9246 achieves its optimum performance when it is driven differentially. The ADA4938 eliminates the need for a transformer to drive the ADC, performs a single-ended-to-differential conversion, buffers the driving signal, and provides appropriate level shifting for dc coupling.

The ADA4938 is configured with dual ±5 V supplies and a gain of ~2 V/V for a single-ended input to differential output. The 76.8 Ω termination resistor, in parallel with the single-ended input impedance of 137 Ω, provides a 50 Ω dc termination for the source. The additional 30.1 Ω (120 Ω total) at the inverting input balances the parallel dc impedance of the 50 Ω source and the termination resistor driving the noninverting input.

The signal generator has a symmetric, ground-referenced bipolar output. The V_{OCM} pin of the ADA4938 is connected to the CML pin of the AD9246 to set the output common-mode level at the appropriate point. A portion of this is fed back to the summing nodes, biasing –IN and +IN at 0.55 V. For a common-mode voltage of 0.9 V, each ADA4938 output swings between 0.4 V and 1.4 V, providing a 2 V p-p differential output.

The output is dc-coupled to a single-pole, low-pass filter. The filter reduces the noise bandwidth of the amplifier and provides some level of isolation from the switched capacitor inputs of the ADC. The AD9246 is set for a 2 V p-p full-scale input by connecting the SENSE pin to AGND. The inputs of the AD9246 are biased at 1 V by connecting the CML output, as shown in Figure 69.

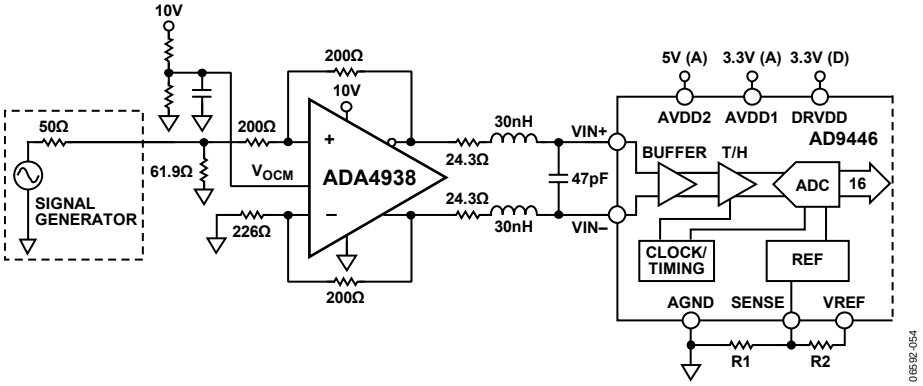

Figure 68. ADA4938 Driving an AD9446, 16-Bit, 80 MSPS ADC

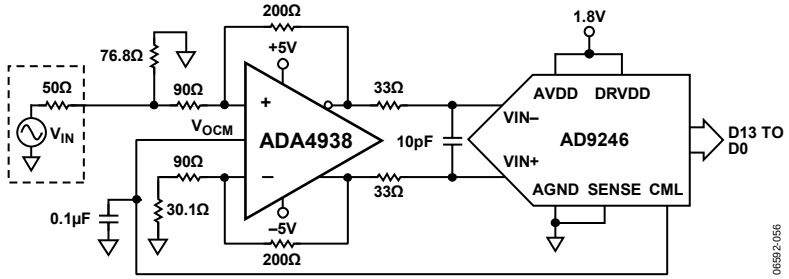

Figure 69. ADA4938 Driving an AD9246, a 14-Bit, 125 MSPS ADC

OUTLINE DIMENSIONS

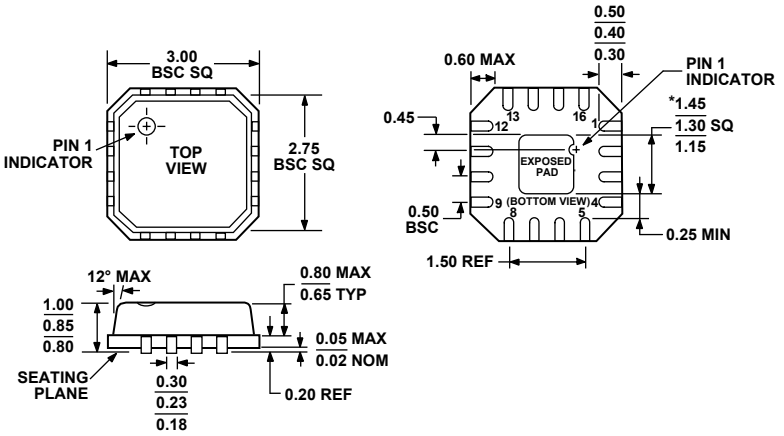

Figure 70. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm × 3 mm Body
(CP-16-2)
Dimensions shown in millimeters

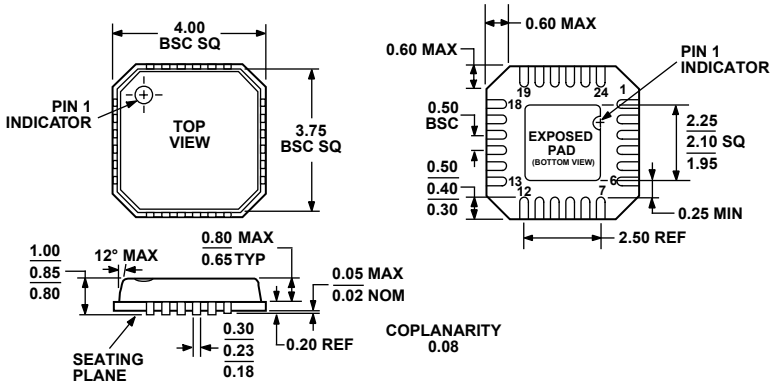

Figure 71. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-24-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADA4938-1ACPZ-R2[1]	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-2	5,000	H11
ADA4938-1ACPZ-RL[1]	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-2	1,500	H11
ADA4938-1ACPZ-R7[1]	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-2	250	H11
ADA4938-2ACPZ-R2[1]	−40°C to +85°C	24-Lead LFCSP_VQ	CP-24-1	5,000	
ADA4938-2ACPZ-RL[1]	−40°C to +85°C	24-Lead LFCSP_VQ	CP-24-1	1,500	
ADA4938-2ACPZ-R7[1]	−40°C to +85°C	24-Lead LFCSP_VQ	CP-24-1	250	

[1] Z = RoHS Compliant Part.

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